

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A switch circuit comprising:

an input terminal which receives an input signal;

an internal circuit which executes a predetermined function;

a first MOS transistor of a first conductivity type which is coupled between the input terminal and the internal circuit, and which has a control gate receiving a control signal, a first electrode coupled to the input terminal, and a second electrode; [[and]]

a second MOS transistor of a second conductivity type that is opposite the first conductivity type, the second MOS transistor being coupled between the input terminal and the internal circuit, and having a control gate receiving a signal having a phase opposite the control signal, a first electrode coupled to the second electrode of the first MOS transistor, and a second electrode coupled to the internal circuit;

another internal circuit which executes another predetermined function; and

a switch element which is coupled between the input terminal and the another internal circuit, and which has a control gate receiving the control signal, a first electrode coupled to the input terminal, and a second electrode coupled to the another internal circuit,

wherein the internal circuit is an analog circuit and the another internal circuit is a digital circuit.

Claim 2 (Previously Presented): The switch circuit according to Claim 1, wherein the first MOS transistor is an n-type MOS transistor and the second MOS transistor is a p-type MOS transistor.

Claim 3 (Original): The switch circuit according to Claim 2, wherein the second MOS transistor has a substrate terminal connected to the second electrode of the second MOS transistor.

Claim 4 (Currently Amended): The switch circuit according to Claim 1, wherein the first MOS transistor is a p-type MOS transistor and the [[a]] second MOS transistor is an n-type MOS transistor.

Claim 5 (Original): The switch circuit according to Claim 4, wherein the first MOS transistor has a substrate terminal connected to the second electrode of the first MOS transistor.

Claims 6-7 (Canceled)

Claim 8 (Currently Amended): A switch circuit comprising:

- an input terminal receiving an input signal;
- a first internal circuit having a first noise resistance capability;
- a second internal circuit having a second noise resistance capability that is weaker than the first noise resistance capability;
- a ~~switch~~ switching circuit connected between the input terminal and the first internal circuit, the ~~switch~~ switching circuit having a control terminal receiving a control signal;
- a first MOS transistor of a first conductivity type having a control gate receiving the control signal, a first electrode connected to the input terminal and a second electrode; and
- a second MOS transistor of a second conductivity type that is opposite the first conductivity type, the second MOS transistor having a control gate receiving an inverted signal having a phase opposite the control signal, a first electrode connected to the second electrode of the first MOS transistor and a second electrode connected to the second internal circuit.

Claim 9 (Currently Amended): The switch circuit according to Claim 8, wherein the ~~switch~~ switching circuit is a transfer gate having a PMOS transistor and an NMOS transistor connected in parallel.

Claim 10 (Previously Presented): The switch circuit according to Claim 8, wherein the control signal is a test signal.

Claim 11 (Previously Presented): The switch circuit according to Claim 8, wherein the first internal circuit is a digital circuit and the second internal circuit is an analog circuit.

Claim 12 (Previously Presented): The switch circuit according to Claim 8, wherein the control signal is input through another terminal.

Claim 13 (Previously Presented): The switch circuit according to Claim 8, further comprising an inverter having an input terminal receiving the control signal and an output terminal outputting the inverted signal.

Claim 14 (Previously Presented): A switch circuit comprising:

- an input terminal receiving an input signal;
- a control input terminal receiving a control signal;
- a first internal circuit having a first noise resistance capability;
- a second internal circuit having a second noise resistance capability that is weaker than the first noise resistance capability;
- a first switch circuit connected to the input terminal, the control input terminal and the first internal circuit, the first switch circuit passing the input signal to the first internal

circuit responsive to the control signal; and

a second switch circuit connected to the input terminal, the control input terminal and the second internal circuit, the second switch circuit passing the input signal to the second internal circuit responsive to the control signal, the second switch circuit including

a first MOS transistor of a first conductivity type having a control gate receiving the control signal, a first electrode connected to the input terminal and a second electrode, and

a second MOS transistor of a second conductivity type that is opposite the first conductivity type, the second MOS transistor having a control gate receiving an inverted signal having a phase opposite the control signal, a first electrode connected to the second electrode of the first MOS transistor and a second electrode connected to the second internal circuit.

Claim 15 (Previously Presented): The switch circuit according to Claim 14, wherein the first switch circuit is a transfer gate having a PMOS transistor and an NMOS transistor connected in parallel.

Claim 16 (Previously Presented): The switch circuit according to Claim 14, wherein the control signal is a test signal.

Claim 17 (Previously Presented): The switch circuit according to Claim 14, wherein the first internal circuit is a digital circuit and the second internal circuit is an analog circuit.

Claim 18 (Previously Presented): The switch circuit according to Claim 14, further comprising an inverter having an input terminal receiving the control signal and an output terminal outputting the inverted signal.